In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Previously presented) An integrated circuit component comprising:

a logic block capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of a system bus; and

a logic block capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the system bus, wherein the first companion integrated circuit and the second companion integrated circuit are disposed in separate integrated circuit chips.

2. (Previously presented) The integrated circuit component of claim 1, further comprising a unified bus logic block configured to consolidate information received from both logic blocks.

3. (Previously presented) The integrated circuit component of claim 1, further comprising a functional logic block for performing at least one logic operation for the integrated circuit component.

4. (Original) The integrated circuit component of claim 1, wherein the system bus is a point-to-point serial communication bus.

5. (Original) The integrated circuit component of claim 1, wherein the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus.

6. (Previously presented) A system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component, comprising:

a host integrated circuit component communicating with other integrated circuit components via a system bus;

a first integrated circuit component comprising logic for interfacing with a first portion of system bus;

a second integrated circuit component comprising logic for interfacing with a second portion of system bus;

a third integrated circuit component not directly coupled with the system bus and comprising logic for communicating with the host integrated circuit via the first and second integrated circuit components, wherein the first integrated circuit component, the second integrated circuit component, and the third integrated circuit component are provided in separate integrated circuit chips.

7. (Original) The system of claim 6, further at least one additional integrated circuit component not directly coupled with the system bus, and comprising logic for communicating with the host integrated circuit via the first, second, and third integrated circuit components.

8. (Previously presented) The system of claim 6, wherein the third integrated circuit further comprising a functional logic block that performs a conventional functional operation.

9. (Previously presented) An integrated circuit component comprising:

a first set of conductive pins for channeling communications to a host integrated circuit through a first intermediate integrated circuit, the first intermediate integrated circuit being in direct communication with the host integrated circuit via a first portion of a system bus; and

a second set of conductive pins for channeling communications to the host integrated circuit through a second intermediate integrated circuit, the second intermediate integrated circuit being in direct communication with the host integrated circuit via a second portion of the system bus, wherein the integrated circuit component, the first intermediate integrated circuit and the second intermediate integrated circuit are provided in separate integrated circuit chips.

10. (Previously presented) The integrated circuit component of claim 9, further comprising unified bus logic configured to consolidate information received from the channeled communications through the first and second set of conductive pins.

11. (Previously presented) An integrated circuit component comprising two independent logic portions, each logic portion being capable of being alternatively configured to communicate with a host integrated circuit via a portion of a system bus and a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a portion of a system bus.

12. (Previously presented) The integrated circuit component of claim 11, further comprising a unified bus logic block configured to consolidate information received from both logic portions.